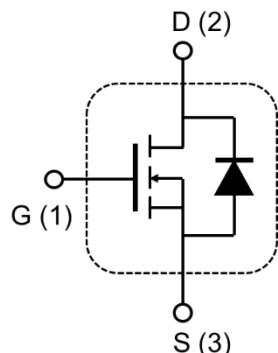


TSC065F050

Silicon Carbide Power MOSFET

N-CHANNEL ENHANCEMENT MODE

TO-247-3L**Inner Circuit****Product Summary**

V_{DS}	650V
I_{D(@25°C)}	52A
R_{DS(on)}	50mΩ

**Features**

- ◆ Low On-Resistance and Capacitance
- ◆ AEC-Q101 Qualified
- ◆ Avalanche Ruggedness
- ◆ Halogen Free, RoHS Compliant

Applications

- ◆ SMPS / UPS / PFC
- ◆ EV Charging station & Motor Drives
- ◆ Power Inverters & DC/DC Converters
- ◆ Solar/ Wind Renewable Energy

Benefits

- ◆ Higher System Efficiency
- ◆ Parallel Device Convenience
- ◆ High Temperature Application
- ◆ High Frequency Operation

Maximum Ratings (T_c=25°C)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	V _{DS, max}	V _{GS} =0V, I _D =100μA	650	V
Continuous Drain Current	I _D	V _{GS} =20V, T _C =25°C	52	A
		V _{GS} =20V, T _C =110°C	31	
Pulse Drain Current	I _{D, pulse}	t _{PW} limitation per Fig.17	119	
Avalanche energy, Single Pulse	E _{AS}	V _{DD} =100V, I _D =10A	1250	mJ
Power Dissipation	P _D	T _C =25°C	208	W
Recommend Gate Source Voltage	V _{GS, op}	Static	-5/+20	V
Maximum Gate Source Voltage	V _{GS, max}	AC (f > 1Hz)	-10/+25	
Junction & Storage Temperature	T _j , T _{stg}		-55/+150	°C
Soldering Temperature	T _L		260	

Electrical Characteristics ($T_j=25^\circ\text{C}$)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{DS}}=100\mu\text{A}$	650			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=10\text{V}, I_{\text{DS}}=10\text{mA}$		2.6		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}$		<1	50	μA
		$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}$ $T_j=150^\circ\text{C}$		5	200	
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=20\text{V}, V_{\text{DS}}=0\text{V}$			250	nA
Drain-Source On-State Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=20\text{V}, I_{\text{DS}}=30\text{A}$		50	65	$\text{m}\Omega$
		$V_{\text{GS}}=20\text{V}, I_{\text{DS}}=30\text{A},$ $T_j=150^\circ\text{C}$		65		
Input Capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=400\text{V}$ $f=1\text{MHz}, V_{\text{AC}}=25\text{mV}$		1850		pF
Output Capacitance	C_{oss}			208		
Reverse Transfer Capacitance	C_{rss}			33		
Effective Output Capacitance, Energy Related	$C_{\text{o(er)}}$	$V_{\text{GS}}=0\text{V},$ $V_{\text{DS}}=0 \text{ to } 400\text{V}$		237		
Effective Output Capacitance, Time Related	$C_{\text{o(tr)}}$	$I_D=\text{const.}, V_{\text{GS}}=0\text{V},$ $V_{\text{DS}}=0 \text{ to } 400\text{V}$		305		
Turn On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DS}}=400\text{V},$ $V_{\text{GS}}=-4/+20\text{V},$ $I_D=20\text{A}, R_L=20\Omega,$ $R_{\text{G(ext)}}=2.7\ \Omega$		16		ns
Rise Time	t_r			17		
Turn Off Delay Time	$t_{\text{d(off)}}$			20		
Fall Time	t_f			10		
C_{oss} Stored Energy	E_{oss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=400\text{V}$ $f=1\text{MHz}, V_{\text{AC}}=25\text{mV}$		24		μJ
Turn-on Switching Energy	E_{on}	$V_{\text{DS}}=400\text{V},$ $V_{\text{GS}}=0/20\text{V}, I_D=30\text{A},$ $R_{\text{G(ext)}}=2.7\ \Omega$		32*		
Turn-off Switching Energy	E_{off}			40*		
Internal Gate Resistance	$R_{\text{G(int.)}}$	$f=1\text{MHz}, V_{\text{AC}}=25\text{mV}$		1.2		Ω

*Based on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in E_{on} .

Built-in SiC Diode Characteristics ($T_j=25^\circ\text{C}$)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	$V_{\text{GS}}=-5\text{V}, I_{\text{SD}}=5\text{A}$	4.1	V
Continuous Diode Forward Current	I_s	$V_{\text{GS}}=-5\text{V}, T_c=25^\circ\text{C}$	36	A
Reverse Recovery Time	t_{rr}	$V_{\text{GS}}=0\text{V},$ $I_{\text{SD}}=30\text{A}, V_{\text{DS}}=400\text{V},$ $di/dt=300\text{A}/\mu\text{s}$	58	ns
Reverse Recovery Charge	Q_{rr}		122	nC
Peak Reverse Recovery Current	I_{rrm}		3.75	A

Gate Charge Characteristics ($T_j=25^\circ\text{C}$)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	$V_{DS}=400\text{V}$, $V_{GS}=-5/+20\text{V}$, $I_D=30\text{A}$	30	nC
Gate to Drain Charge	Q_{GD}		43	
Total Gate Charge	Q_G		121	
Gate plateau voltage	V_{pl}		8.8	V

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta,JC}$	0.6	K/W

Typical Device Performance

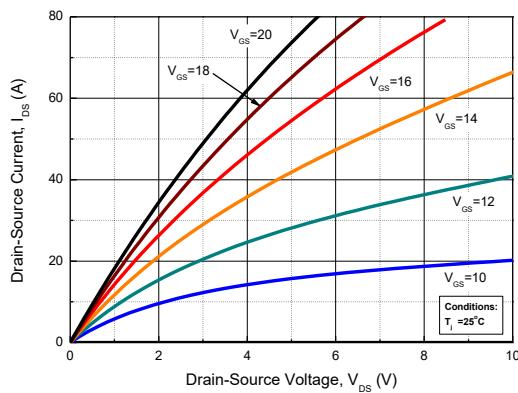


Fig. 1 Forward Output Characteristics at
 $T_j = 25^\circ\text{C}$

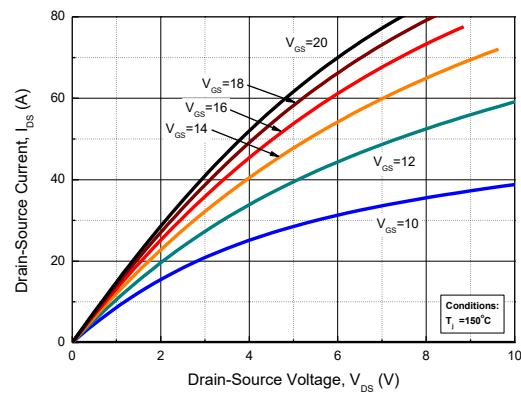


Fig. 2 Forward Output Characteristics at
 $T_j = 150^\circ\text{C}$

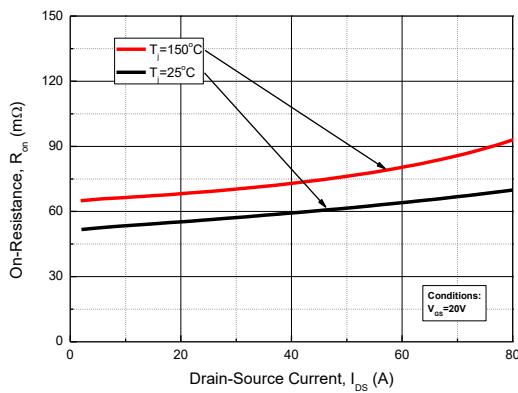


Fig. 3 On-Resistance vs. Drain Current for
Various T_j

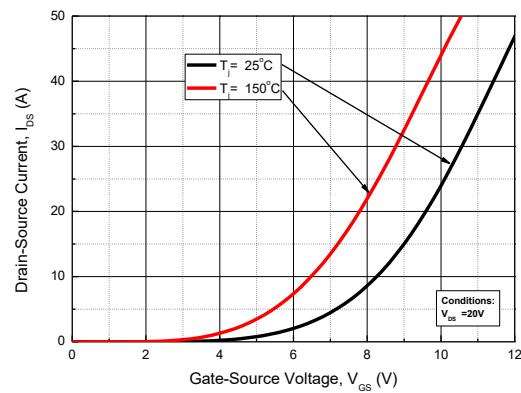


Fig. 4 Transfer Characteristics for Various T_j

Typical Device Performance

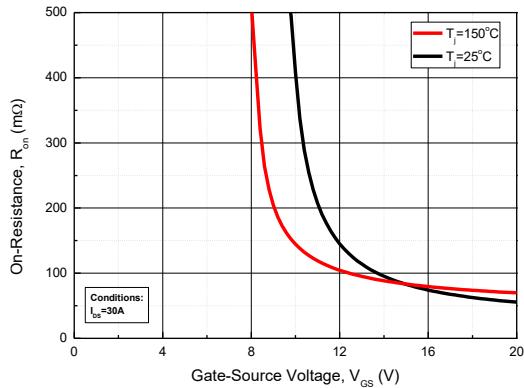


Fig. 5 On-Resistance vs. Gate Voltage for Various T_j

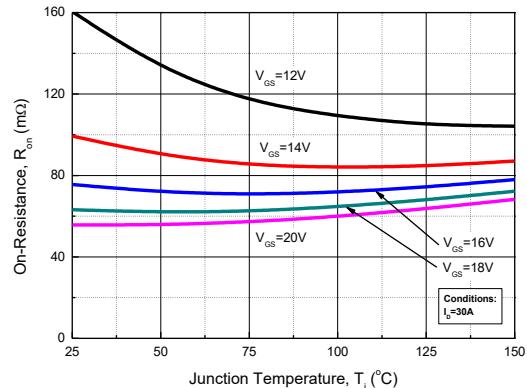


Fig. 6 On-Resistance vs. Temperature for Various Gate Voltage

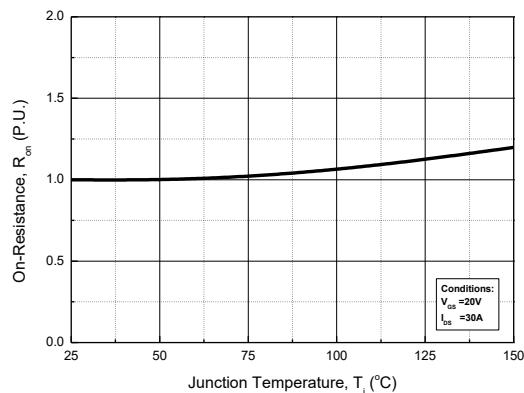


Fig. 7 Normalized On-Resistance vs. Temperature

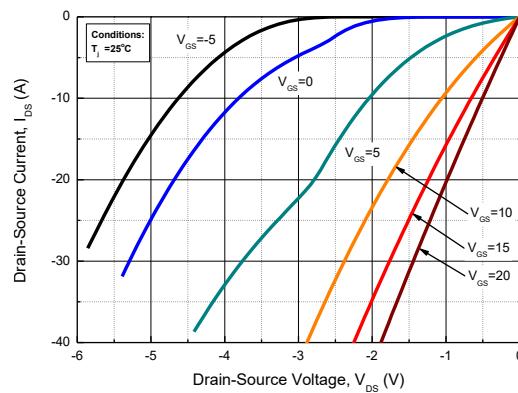


Fig. 8 Reverse Output Characteristics at $T_j = 25^\circ\text{C}$

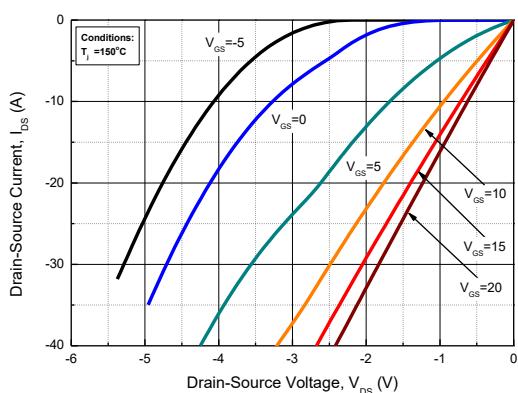


Fig. 9 Reverse Output Characteristics at $T_j = 150^\circ\text{C}$

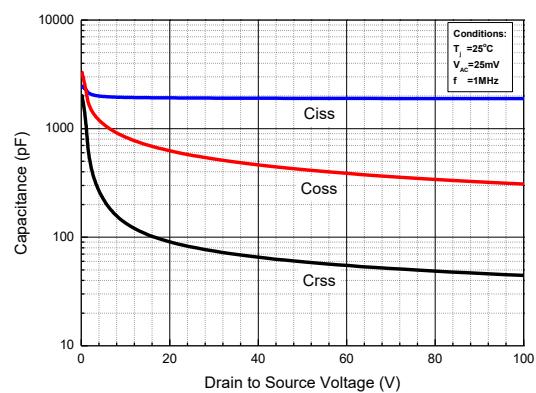


Fig. 10 Capacitances vs. Drain to Source Voltage (0 - 100V)

Typical Device Performance

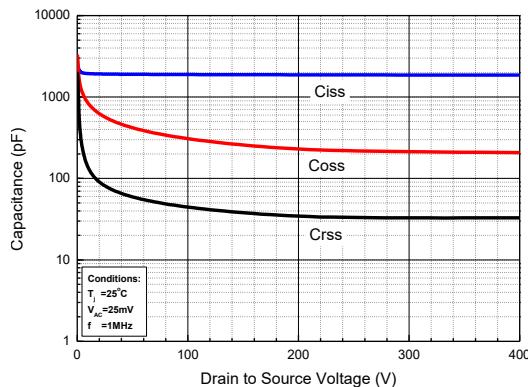


Fig. 11 Capacitances vs. Drain to Source Voltage (0 - 400V)

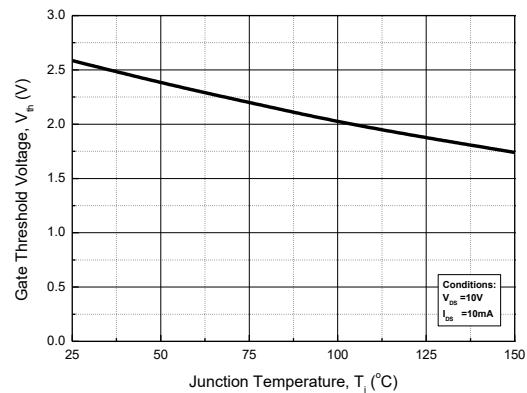


Fig. 12 Threshold Voltage vs. Temperature

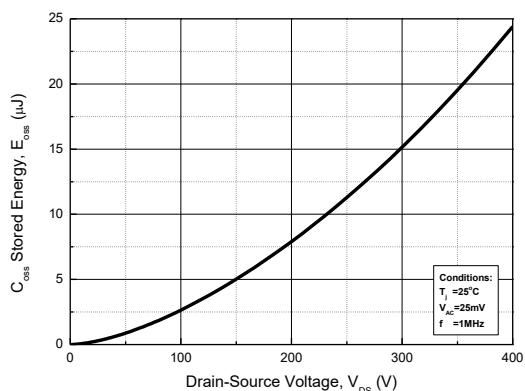


Fig. 13 Output Capacitor Stored Energy*

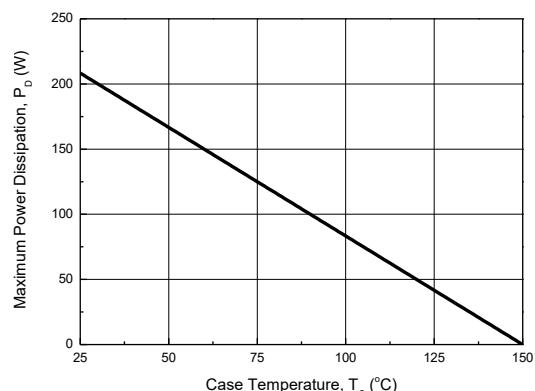


Fig. 14 Maximum Power Dissipation Derating vs. Case Temperature

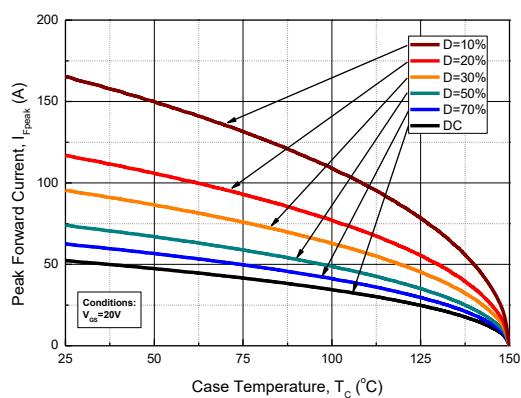


Fig. 15 Drain Current Derating vs. Case Temperature

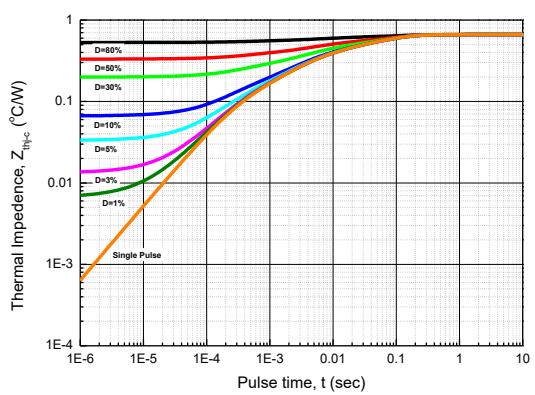


Fig. 16 Transient Junction to Case Thermal Impedance

Typical Device Performance

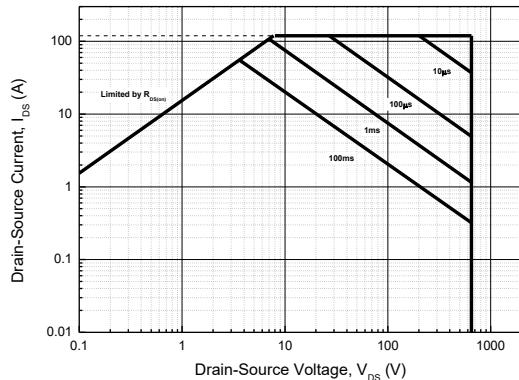


Fig. 17 Safe Operating Area

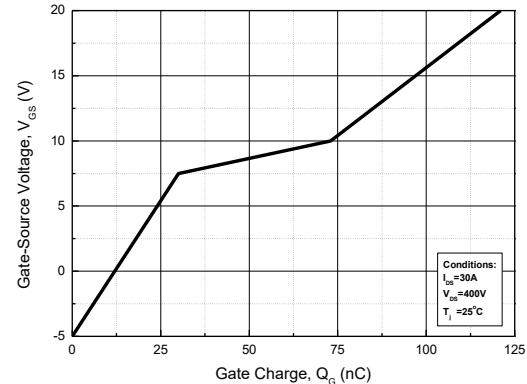


Fig. 18 Gate Charge Characteristics

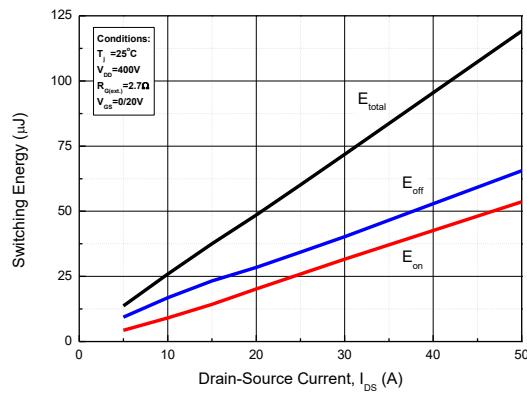


Fig. 19 Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}=400V$)*

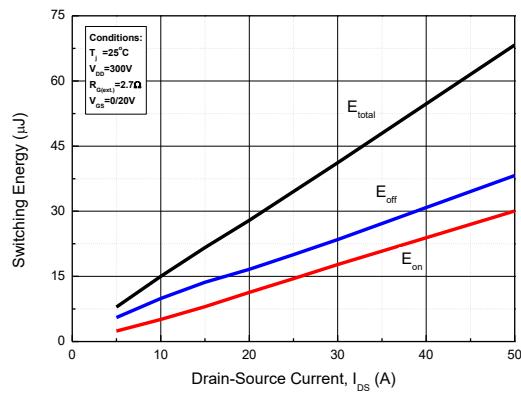


Fig. 20 Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}=300V$)*

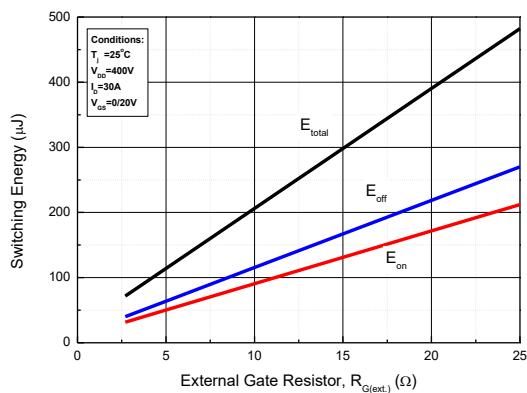
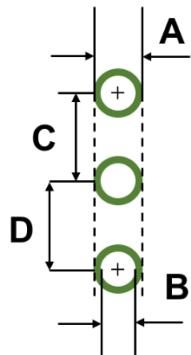


Fig. 21 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)*

*Based on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in E_{on} .

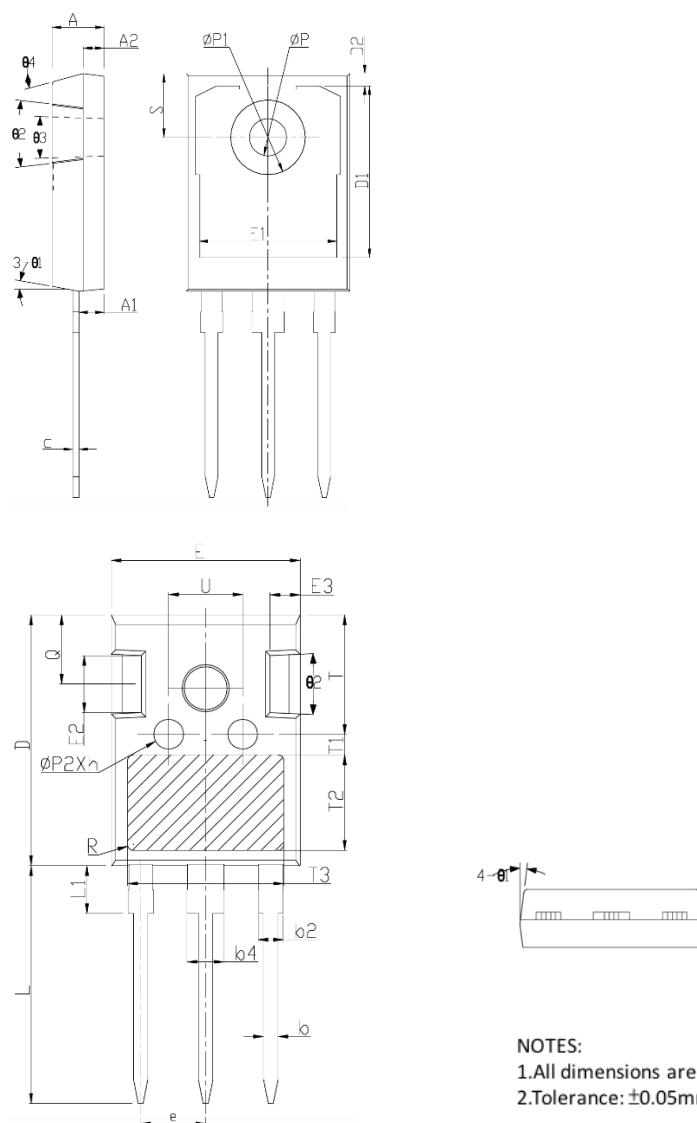
Recommended Solder Pad Layout (TO-247-3L)



Mechanical Parameters

Parameter	Symbol	Typical	Unit
Length	A	3.048	mm
	B	2.032	
	C	5.436	
	D	5.436	

Mechanical Parameters



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	4.75	5.00	5.25
A1	2.16	2.41	2.66
A2	1.85	2.00	2.15
b	1.11	1.21	1.35
b2	1.90	2.01	2.25
b4	2.90	3.01	3.25
c	0.51	0.61	0.75
D	20.60	21.00	21.40
D1	16.15	16.55	16.95
D2	1.00	1.20	1.40
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.70	5.00	5.30
E3	2.25	2.50	2.75
e	5.44BSC		
h	0.00	0.10	0.25
L	19.52	19.92	20.32
L1	-	-	4.30
ΦP	3.35	3.60	3.85
ΦP1	-	-	7.30
ΦP2	2.25	2.50	2.75
Q	5.50	5.80	6.10
S	6.15BSC		
R	0.50REF		
T	9.70	-	10.30
T1	1.65REF		
T2	8.00REF		
T3	12.80REF		
U	5.90	-	6.50
θ1	4°	7°	10°
θ2	2°	5°	8°
θ3	1°	-	2°
θ4	10°	15°	20°

*The information provided herein is subject to change without notice.